



Multi Processor Architecture for Automatic Control

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The MUPAAC Project

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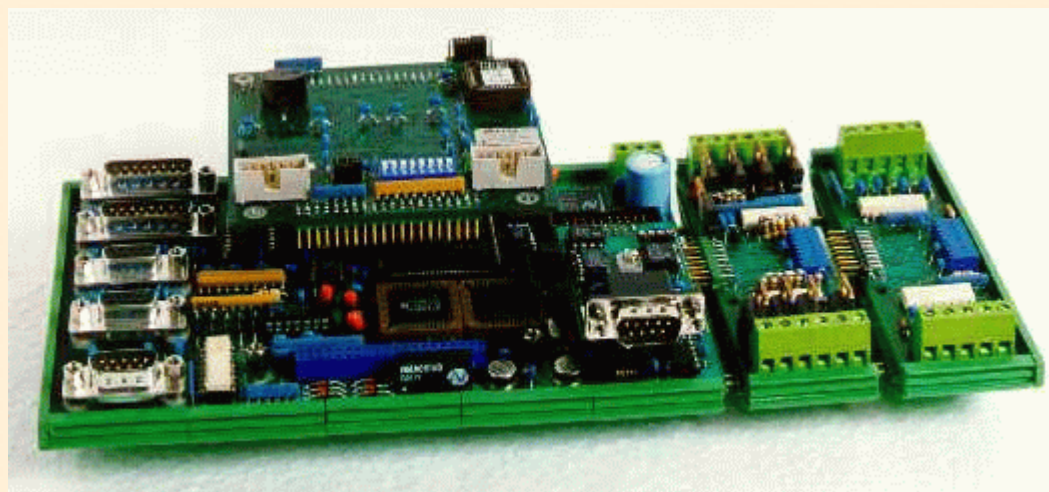
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MUPAAC project consists in improving capabilities of an already present architecture for automatic control for industrial machines. It will make possible to reach performance better or comparable to the best which can be found in the market of automatic controllers at lower cost.

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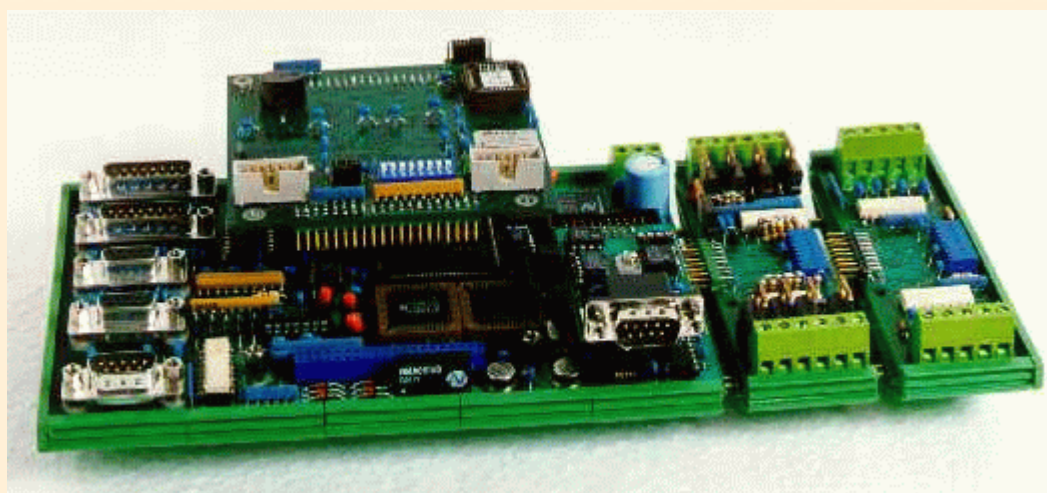
- the adoption of HPCN technology for making performance of microprocessor based controllers of SED comparable or better with respect to the best which are available on the market, but at a lower cost/price for the machine builders. An increment of functionality is also planned;
- introducing HPCN technology for obtaining, on the basis of already available computerized control of SED a flexible and reconfigurable parallel/distributed system for control in order to reduce the costs/prices for the machine builders of about 20 %. The system has been considered strongly needed for integrating automatic machines into pipelines of production;
- the deployment of HPCN technology for improving performance and decreasing of cost of products and thus for covering a wider market;
- the dissemination of results at National and European levels.





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Industrial Benefit

The proposed MUPAAC architectures will be very interesting for the machine builders, since it guarantees the return of the investment for developing the present proposal.

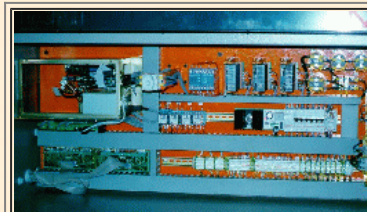
Machine builders are strongly interested to have:

1. *a reduction of cost/price of about the 20 % for the CNC;*
2. *a high flexibility since the same architecture could be used for covering different types of machines, different in performance and complexity;*
3. *a controller which can be integrated in a pipeline of production (FMC line) by means of a fast connection;*
4. *a scalable architecture on which several robots and services can be added even later without restarting from a new CNC but only adding the components needed;*
5. *a set of new functionalities due to the integrability of the machines with the others of the same area.*

The above needs can be satisfied by using HPCN technology for building a flexible multiprocessor architecture for automatic control. Thus, this architecture:

- must be flexible. In the sense that on the basis of the performance required different configurations will be possible with corresponding scalable cost/price for the end-user/machine builders;
- must be less expensive with respect to the typical price of the market, previously reported
- must be connectable with other automatic controls in order to build automated areas.

MUPAAC at Work



[Click to see a more detailed image.](#)



[Click to see a more detailed image.](#)

Success Story

HPCN Reduces Costs of Production Pipelines

SED & VALIANI

A pipeline of production presents several elaboration phases in which the movement of interpolated axes is needed. These activities have to be synchronized with the several other activities and switches along the pipeline. Numerical controls for such a system have to be flexible and strongly expandable since the pipelines are frequently reconfigured and different pipeline may have strongly different technical requirements. MUPAAC project is a solution for implementing flexible architecture for the automatic control of industrial machines. With MUPAAC is possible to reach performance better or comparable to the best which can be found in the market of automatic controllers but at a lower cost/price: a reducing of 23% for the costs of controllers for the machine builders. With MUPAAC SED increased its market by improving performance of controllers. This has been obtained by passing from a simple dual processor architecture to a flexible multiprocessor architecture with the introduction of HPCN technology.

[Click here to see or download the compressed full Word 97 version of success story \(2Mb\)](#)

General Background

With MUPAAC activity, the partners intend to improve the capabilities of the already produced architecture (INDEX-DSP of SED employed by VALIANI on their machines) for automatic control of industrial machines. This will make possible to reach performance better or comparable to the best that can be found in the market of automatic controllers at a lower cost.

Presently, most of the automatic machine tool (for milling, cutting, measuring, moving, soldering, electron erosion, etc.) which are used in pipelines of production are controlled by microprocessor based systems. These are usually called CNC (Computerized Numerical Control).

The automated systems of production can be classified in three main categories. The first is usually defined as FMM (Flexible Manufacturing Module) {Montanelli96}. These are constituted by a single machine tool, for example a working center to which auxiliary robots for charging and discharging parts and tools, are added. Moreover, sometimes also measuring machines complete the area. The FMM control consists in a single microprocessor based system that coordinates the machines and the auxiliary tools and services (e.g., 3 axes for the machine and 2-3 axes for each robot of service). The second category is the FMC (Flexible Manufacturing Cell), it constitutes the core of several FMM modules. These are connected by automatic mechanisms for transferring pieces among FMMs etc. The production process management of the cell is managed by a central control unit. All FMMs of the FMC have their own controllers which talks to the central processor by means of a local communication network. In this case the number of axes can be, as a limit, even 64; thus, 3-4 for each CNC.

A further factory's automation model is the FMS - Flexible Manufacturing System. It represents the consecutive level of the production cell in the development of the production and diversification capability of an industrial plant. It is made by more production cells which are connected with a central data processor which manages besides the various production cells also the production flow control, for example orders and stock house supplies. A quick analysis made by the distributors of the most important numerical control producers shows encouraging results for starting a research in this field. Among the most important CNC's producers only SIEMENS owns a network based on international standards IEE 802.3 (CSMA/CD), which allows to link each other more axes controllers. In this case, the communication among controllers and process management computers occurs through some bridges that connect each other the controllers network with that (token ring type) of the process management data processors. Many others firms such as OMRON, ABB, Blue Chip own communication networks which connect each others only PLC modules. The American enterprise Intelligent Instrumentation uses an Ethernet network to connect its own field bus modules such as Profibus, Bitbus or CANbus. These connection types are Master-slave, that is to say that the Master manages the communication, typical centralized non distributed controller. The electronic systems produced by SED are mainly used for the machines management which belong to the first type, FMM, and in lower quantity also on FMC systems. Recently there is an international strong request for the realization of FMC and FMS systems.

In general, a CNC system receives the instructions describing the elaboration to be performed in terms of an ISO program. These are generated by CAD/CAM stations on the basis of tools used on the machine and considering many other details. The ISO program is composed of elementary instructions (usually called blocks), and each block may include instructions to coordinate the macropoints for interpolation (plus eventually some technical information). The CNC system, by using the interpolator, calculates the micropoints that are useful to generate the profile required between the given macropoints. The operation of a CNC can be summarized as follows:

- Interpretation of ISO programs coming from (i) the console, (ii) diskettes, (iii) a network connection, for translating each instruction in low-level commands. Specific versions of ISO programs can be used for both describing the operation to be made by the machine and by its I/O ports by using logic equations;

- **Execution of low-level commands for axes of the machines and for the other auxiliary services by means of several digital and analog input/output ports; these are usually called in short "I/O ports";**
- **CNC controls the execution of each command and action by using the information coming from the machine by means of sensors, etc.**

The CNC is capable of detecting errors/faults that may occur on the machine. These are corrected by special set of instructions and/or are reported towards the other microprocessor based systems which are monitoring all the automated area according to FMC policy.

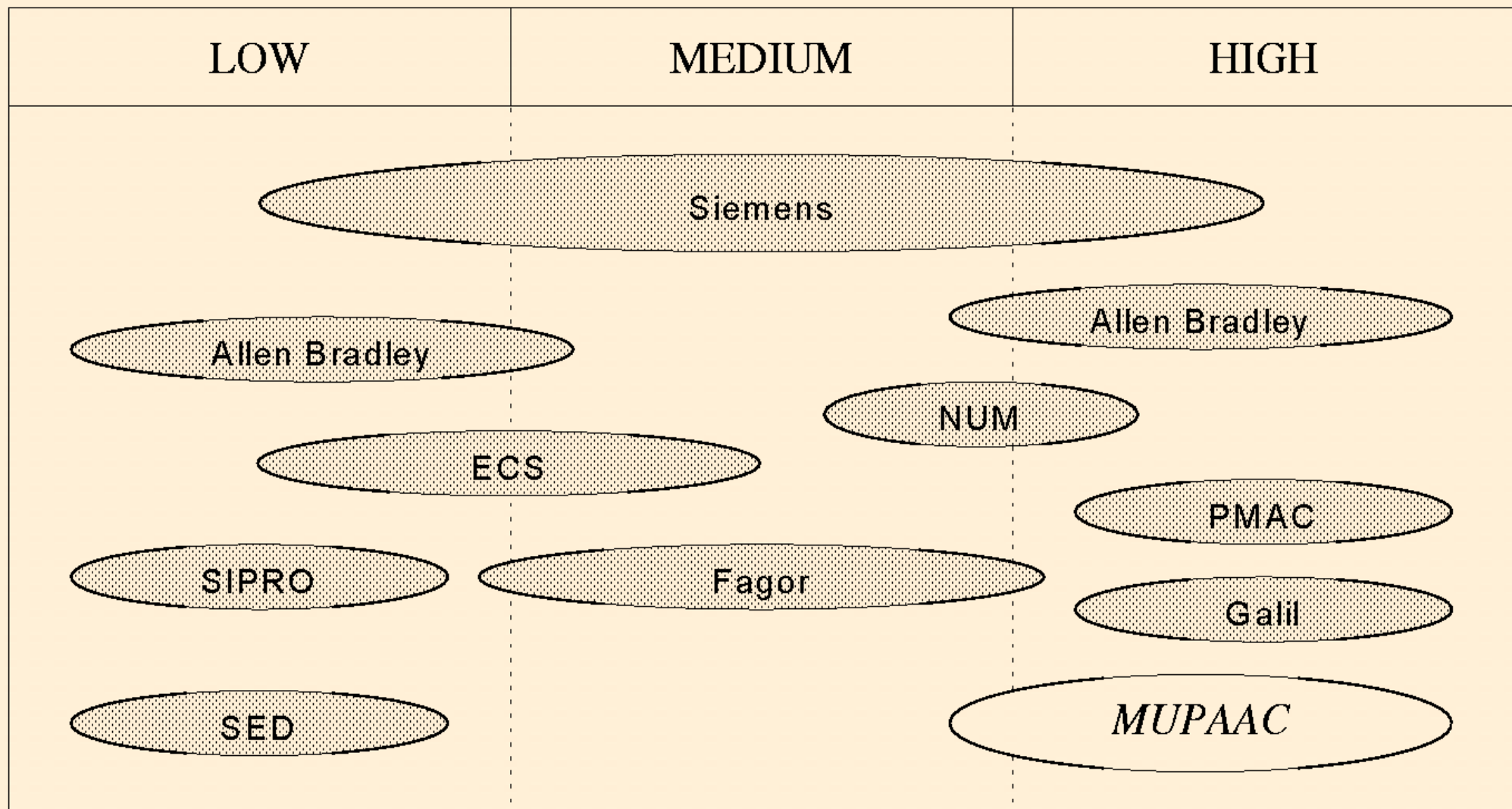
In the specific field of builders for cutting machines for producing passpartout (as VALIANI, end user partner of this project) (e.g., ZUND, Swiss, Gunnar, Swiss), the machines can be integrated in FMC areas only by means of slow communication supports (e.g., RS232). These machines are also critically served by robots for loading pieces and/or tools.

Market Situation

In Europe there exists more than 7500 automatic machine builders. All these builders produce about 500000 complex machines per year (more than 8 axes), these are installed in all world (information coming from UCIMU and CECIMO, Italian and European association of machine builders, respectively).

In the market, there exists several builders of CNC; some of them are strongly oriented to support FMM architectures. Those which are capable of controlling FMC areas can be classified in three main categories on the basis of the refresh time (period) for evaluating/generating the actions on axes, Ref.Ax. For lower values of Ref.Ax. we have higher performance and costs, since a short refresh time leads to reduce errors (in cutting, soldering, etc., i.e., in following the planned profile) and executing elaborations in shorter time. In Fig.1 a schema presenting the classification of control builders is shown. According to our market analysis, which has been performed by interviewing machine builders, studying related documents, making direct questions at fairs, and by performing direct experiments, the following features have been identified:

- **HIGH performance controllers/market (Ref.Ax < 1msec):** PMAC (USA), GALIL (Israel), Allen Bradley (USA), Siemens (Germany), NUM (France), etc. In this case, the price is about 725 Ecus per axis.
- **MEDIUM performance controllers/market (with 1 msec < Ref.Ax <7 msec):** Fagor (Spain), Siemens (Germany), etc. In this case, the price is about 420 Ecus per axis.
- **LOW performance controllers/market (with Ref.Ax 7 msec).** SIPRO (Italy), SED with INDEX-DSP architecture (Italy), ECS (Italy), Siemens (Germany), etc. In this case, the price is about 300 Ecus per axis or less



Please note that some firms present several types of solutions which are capable of covering different sectors or the market -- e.g., Siemens, ECS, etc. Presently the controllers which are employed on cutting, soldering, moving, machine tools belong typically to MEDIUM and LOW categories. The adoption of high performance will improve the precision of elaboration allowing the adoption of more complex tools such as lasers, elaborations directly at the final resolution on milling machines, etc.

All the above mentioned architectures are quite modular, in the sense that most of them present a simple module for managing the single CNC/FMM, with eventually all its services. On the other hand, for implementing FMC architectures, some of them use communication networks, while other adopt mechanisms for synchronizing single FMM by using connections among digital I/O ports. For all the above mentioned solutions the price is quite proportional with the number of axes as highlighted in the above list of items.

Presently the complexity of FMC is growing since they need a higher number of robots and services. Some of these services need of many axes for their control. This local complexity of control cannot be managed by using decentralized numerical controllers since the remote connection by means of serial or specific channels is not fast enough {Raji94}, see <http://www.synergic.com>. For these reasons, some builders are improving the capabilities of their CNCs by increasing the power of the microprocessor. This augments the final price of the CNCs.

More recently, few builders of numerical controls in USA are beginning to build strictly coupled multiprocessor-based systems (parallel architectures) for implementing flexible CNCs and FMCs. This flexibility also reduces the cost/price of complex numerical controls and increase the modularity of the system.

For these reasons SED intends to transform its INDEX-DSP architecture in a multiprocessor architecture by using HPCN technology. These operations will allow to the new architecture of SED to cover a wider market and to reduce the cost/price of the product, even with respect other products, comparable performance, which are present in the market {Raji94}, see <http://www.synergic.com>.

INDEX-DSP of SED is a dual processor architecture in which a processor is devoted to interpreting ISO programs and generating macropoints while the other is a DSP (Digital Signal Processor) devoted to generating micropoints and controlling axes. The new architecture of SED, called MUPAAC, will be a multi DSP architecture in which a set of DSP boards will be connected to the main board by using a high performance bus.

Technical State of the Art

In the previous paragraphs, the technical state of the art of this sector has been reported.

Please note that, in the field of automatic controllers, there exists several European projects:

- **OSACA and OSACA II (Open System Architecture for Controls within Automation Systems),**
- **MOSAIC (Modular Open System Architecture for Industrial Motion Control) n.5292,**
- **[ICCOC \(Integrating CAD/CAM Operations into CNC-Based Machines\),](#)**
- **PLENT (Planning Small Medium Enterprise Networks) n.20723,**
- **NetCIM (Cooperative Network for CIME Technologies in Europe) n.9901,**
- **AITIME (Advanced Information Technology in Manufacturing Engineering) n.9902.**

For our knowledge only OSACA and MOSAIC have addressed the problem of parallel architectures for control, unfortunately by defining high cost and too complex architectures to be profitably used for low cost systems.

MUPAAC project will take into account the main results produced by these projects. Please note that MUPAAC is a flexible, reconfigurable, multiprocessor architecture based on PCI and DSP. This is a quite new idea.

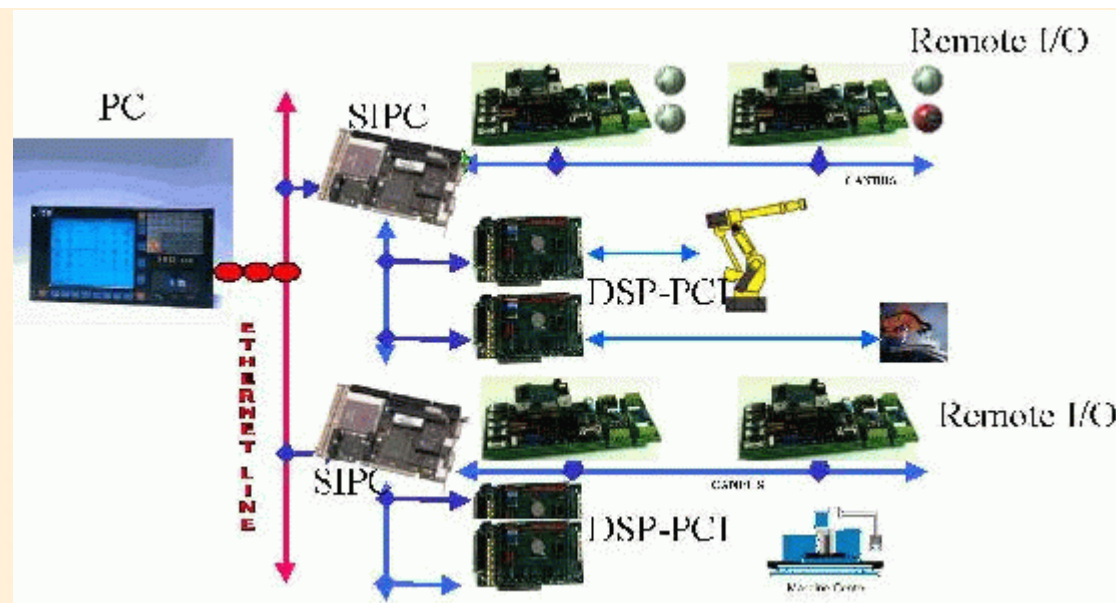
The relationships with the rest of European projects (ICCOC, PLENT, NetCIM, AITIME, etc.) is a mere concept since all these projects are mainly focussed on the integration of controlled areas by means of networks according to a CIM policy.

MUPAAC General Architecture

A prototype of MUPAAC architecture for automatic control will be implemented by using HPCN technologies: parallel architecture, distributed system, communications, control networks, multi-microprocessor architecture; thus the name MUPAAC: Multi Processor Architecture for Automatic Control. The implementation of the MUPAAC prototype involves both hardware and software aspects (see Figs.2 and 3).

The components of MUPAAC system, as reported in Fig.2, are:

- **PC (Personal Computer):** a personal computer which in practical is the user interface of the entire system and the interface towards other areas by means of a Fast Ethernet network. It sends/receives messages to/from the actual microprocessor based systems by means of the TCP/IP-based network or a CANBUS network. For this reason PC can be endowed with a CANBUS board for interface (PC-CANBUS board) or may present an Ethernet card.
- **SIPC board (SED Industrial Peripheral Computer):** a microprocessor based system which interprets ISO instructions coming from PC and manages their execution. The communication with the PC will be implemented by using CANBUS. SIPC also interacts with (i) the DSP-PCI boards for driving axes and receiving alarms and synchronization; (ii) the I/O boards for activating and receiving I/O signals;
- **DSP-PCI boards:** boards based on a DSP, Digital Signal Processor, for managing up to 4 axes by using an improved PID for evaluating the action of motors. For the physical (low) level, the communication between SIPC and its DSP-PCI boards will be made by using a standard PCI bus;
- **I/O boards:** boards which allow the effective acquisition and production of actions on the machine by reading/writing I/O ports. They are endowed with a microprocessor for interpreting messages sent on CANBUS which are specific commands for managing I/O ports;
- **CANBUS:** a communication support used for establishing communications: (i) between the PC and the SIPC boards, and (ii) between each SIPC and its I/O boards;
- **PCI BUS:** a communication support used by each SIPC board for communicating with its DSP-PCI boards.
- **TCP/IP-based Network:** a classical Ethernet or Fast Ethernet network based on TCP/IP. This network support is used when from the PC and SIPCs of the architecture has to pass more than a 500 Kbps.



MUPAAC activity plans to adapt the INDEX-DSP architecture of SED. In particular, this action will consist in improving INDEX-DSP performance and functionalities by using HPCN technologies: removing the LOGIPACK, RS232, RS 485 and the dual port memory communication supports and substituting them with the more efficient mechanisms such as CANBUS and PCI protocols. The adaptation of INDEX-DSP will be an efficient support for focussing this project on technology transfer. For these reasons:

- PC-CANBUS board will be designed and implemented;
- SIPC board for the prototype will be obtained by using commercial products. Its further evolution will be obtained by adapting the INDEX-DSP main board of SED, introducing SIPC-PCI interfaces. Boards for communicating with CANBUS and for Ethernet will be implemented and acquired, respectively. CANBUS board is based on PC104 interface.
- DSP-PCI board will be obtained by adapting the DSP board of INDEX-DSP architecture of SED by introducing the possibility of having a flexible and reconfigurable multi DSP architecture and adding a PCI interface and other features.
- I/O boards will be obtained by adapting I/O boards of SED introducing on these boards an I/O-CANBUS interface (substituting LOGIPACK and RS485).
- CANBUS: is a high-level CANBUS protocol between PC and SIPC boards as well as between SIPC and I/O boards will be defined and development.
- PCI BUS: is a high-level PCI protocol between SIPC and DSP-PCI boards will be defined and development.
- TCP/IP-based Network: is a high-level protocol based on classical API which are available for TCP/IP.

The adaptation of INDEX-DSP hardware/software towards a multiprocessor architecture will consists in removing old parts and adding new communication supports. New functionalities due to the possibility of building a flexible distributed/parallel system for automatic control will be implemented. Therefore, software support for integrating SIPCs along the network and monitoring the network behavior will be implemented by using HPCN technology. This software will be integrated in the already mature software architecture of SED (see Fig.3). Applicative software for generating ISO programs, interpreters, resolver of logic equations, algorithms of control, interpolators, user interface and high-level end-user-oriented applicative software, etc. will be directly inherited by the SED software architecture and collection of products.

For these reasons, a great work will be performed by adapting hardware and software and by integrating the new components (communication supports) into the general architecture. The complete system will reach a greater value with respect to INDEX-DSP, since a new set of strongly innovative products with a set of new functionalities and higher performance will be implemented. In the [component section](#), details about the main components of MUPAAC are reported.

CANBUS: hardware and software issues

Before to discuss what will be done for this component, it is better to explain why the CANBUS network is capable of satisfying our requirements in terms of performance and thus why we have chosen to use it during the feasibility study of SED and DSI.

As previously pointed out the CANBUS is used in two parts of our architecture: for communications between the PC and the SIPC and between SIPC and its I/O boards.

SIPC-I/O boards CANBUS: hardware and software issues

The connection between SIPC and its I/O boards must provide a band large enough to guarantee a refresh time ≤ 10 msec for all I/O ports. This is good value for high performance CNC based systems.

According to CANBUS low-level protocol a frame containing at most 8 bytes of data is sent by using 129 bits on the bus. For these reasons, on the basis of the previous discussion, if a system has to send 256 bits, these can be sent with 32 frames of 129 bits, for a total of 4128 bits. If a refresh time of 10 msec is chosen then 413 Kbps are needed. The maximum throughput of the CANBUS is equal to 1 Mbps, which satisfies the above extreme conditions. Please note that a higher value of bits could be transmitted by using a higher value of refresh time -- e.g., with 15 msec and the same throughput 384 bits can be refreshed.

For this reason, CANBUS or an other bus having the same or better performance is suitable for a system like MUPAAC which requires the above mentioned number of I/O ports; moreover, CANBUS is the cheapest bus in the category. It is also very open since hardware for its implementation is distributed by several vendors, and software is public (see <http://www.omegas.co.uk/can>, <http://www.ba-karlsruhe.de/automation>, <http://www.csv.warwick.ac.uk>, etc.). The use of CANBUS represents an improvement for INDEX-DSP, where the connection between the master board and I/Os is made by a LOGIPACK (a SED proprietary parallel bus) or by means of RS485. A reason for eliminating:

- LOGIPACK is the fact that it is a parallel bus which is fast enough but it is not capable of reaching high distances, while
- RS485 is too slow to support the refresh in time the required number of I/O ports even if it can be used for longer distances with respect to LOGIPACK.

For communicating between SIPC and I/O boards a specific high-level protocol will be implemented. At lower level, in order to improve CANBUS robustness special CANBUS chips which include the automatic correction of errors (resending and controlling local addresses) will be used. It will be light as possible. The protocol will be defined partially reusing those defined for LOGIPACK and RS485 in the INDEX-DSP.

The CANBUS board for SIPC will be implemented for plugging it on the PC104 bus of the mother board. The PC104 is in practical an ISA bus on an industrial connector.

With the aim to obtain the communication through CANBUS channel, between SIPC card and the I/O modules, it will be necessary to plan and to construct a CANBUS card with bus PC104. In this phase of development of the project, it has been thought that the CANBUS PC104 card does not have to have a CPU of support to the Intel 82527 chip for the communication on this serial bus.

Since the total throughput of the system can be heavily influenced from this type of realization, in a more advanced phase this point will be

reexamined. During this second step of the planning it will be estimated if could be necessary that the PC104 CANBUS card should have also a 80188 CPU, that will concur to leave free the elaboration, and the preparation of the packages to send on CANBUS channel from the CPU of the SIPC.

CANBUS I/O structure:

To obtain a flexible I/O apparatus and to decrease the costs of the total system, it has been considered to realize a device formed from a CPU module with a CANBUS connection channel, and specialist modules connected with the CPU through a SPI channel. This solution allows to obtain I/O devices that follow the necessities of the customer in the more tight way.

PC-SIPC boards CANBUS: hardware and software issues

This connection is mainly used for sending ISO programs to SIPC boards and for exchanging high-level controls among the SIPCs of the architecture.

The workload of this communication support is quite low. For the typical applications in which SED automatic controls are used, an ISO program for 4 axes machines of 250 Kbytes is consumed by the machine/controller in about 15 minutes. This means that a load of 277 bytes per second for each DSP-PCI board with 4 axes is needed. If a SIPC manages 8 DSP-PCI boards with 4 axes each SIPC has to acquire from PC 2216 bytes per second. These are sent on the CANBUS by using frames of 129 bits containing 8 bytes each; thus 277 frames, 35 Kbps are needed. This means that the PC-SIPC CANBUS can support even 12 SIPC boards. In effect, this limit is high since that channel is used also for reporting alarms to the main station and for exchanging messages and synchronization among SIPCs. For these reasons, we intend to limit the number of SIPC boards to 10. The increased number of axes which are present on a pipeline of production and the increased speed of CNCs (for satisfy requests of machine builders) require a corresponding increment in speed of the communications; thus a CANBUS has been preferred rather to maintain the serial communication of INDEX-DSP.

Also in this case, for communicating between PC and SIPCs a specific high-level protocol will be implemented. It will be light as possible. In order to improve CANBUS robustness special CANBUS chips which include the correction of errors will be used.

As a conclusion, CANBUS was chosen because it has a maximum bit rate of 1 Mbps which is satisfactory for the above described applications. Moreover CANBUS is not expensive since the related information is public and many vendors of CANBUS chips are present (the basic software is also public). Please note that, it has been chosen as a support for communicating between PC and SIPCs and between SIPC and I/O boards for saving money in implementing CANBUS interfaces and related software.

Moreover the CANBUS between the PC and SIPC can be substituted with an Ethernet network when the bandwidth required is greater than 500Kbs. In that case the Ethernet card are commercial boards.

Low-Level Protocol for CANBUS

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a very high level of security.

Its domain of application ranges from high speed networks to low cost multiplex wiring.

In automotive electronics, engine control units, sensors, etc. are connected using CAN with bit rates up to 1Mbit/s.

To achieve design transparency and implementation flexibility CAN has been subdivided into different layers:

- the (CAN-)object layer

- **the (CAN-)transfer layer**
- **the physical layer**

The object layer and the transfer layer comprise all services and functions of the data link layer defined by the ISO/OSI model.

The scope of the object layer includes:

- **finding which messages are to be transmitted**
- **deciding which messages are received by the transfer layer actually**
- **providing an interface to the application layer related hardware**

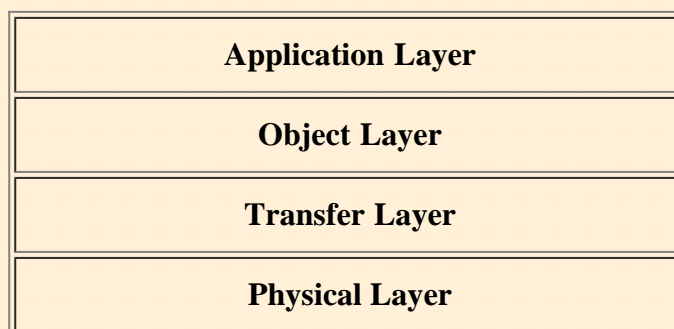
The scope of the transfer layer mainly is the transfer protocol, i.e. controlling framing arbitration, error checking, error signaling, fault confinement. Within the transfer layer it is decided whether the bus is free for starting a new transmission or whether a reception is just starting. Also some general features of the bit timing are regarded as part of the transfer layer.

The scope of the physical layer is the actual transfer of the bits between the different nodes with respect to all electrical properties. Within one network physical layer, of course, has to be the same for all nodes.

CAN has the following properties:

- **prioritization of messages**
- **guarantee of latency times**
- **configuration flexibility**
- **multicast reception with time synchronization**
- **system wide data consistency**
- **multi-master**
- **error detection and signaling**
- **automatic retransmission of corrupted messages as soon as the bus idle again**
- **distinction between temporary errors and permanent failures of nodes and autonomous switching off of defect nodes**

Layered structure of a CAN node:



The Intel 82527 chip was chosen for our CAN module and it will realize the physical, transfer and object layer of this structure. The CAN system it is based on a packetized communication, there was four frame type:

- **DATA Frame**

- **REMOTE Frame**
- **ERROR Frame**
- **OVERLOAD Frame**

Only the DATA frame is visible from the application layer.

High-Level Protocol for CANBUS

In order to resolve the application layer protocol it was analyzed the following standard protocol:

- **Smart Distributed System (SDS) from Honeywell**
- **CAN Open from Can in Automation (CiA)**
- **DeviceNet ODVA from Rockwell**

From these standard protocols for the application layer, it was chosen the SDS one.

The SDS protocol was the smallest, the simplest, and will satisfied all the needs for the applications that will be developed with this CAN bus system. A SDS Network consists of physical components that may be inputs, outputs, PLC interfaces, etc. Physical components are modeled as collections of logical devices that communicate over a physical medium.

The SDS system supports real-time controls, diagnostics and configuration functions for digital and digitized analog, for sensors (inputs) and actuators (outputs). It supports event driven, timed and polled communication modes.

The simplest communication model supported by SDS is the Master/Slaves communication, where the Master device uses the I/O services provided by the Slave devices. The Master views each Slave device as an object with:

- **a set of Attributes that may be read or written;**
- **a set of Actions that may be called;**
- **a set of Events that the device may generate.**

A Slave device is identified by:

- **Device Address (6bit);**
- **EOID (Embedded Object Identifier) (4bit);**

The SDS application layer provides services tailored for the maximum support of a distributed network within the limitations of the CAN Data Link Layer.

The following Application Layer services are available.

Service	Function
Read	Allows ALP (Appl.Layer Protocol) service to read

	a value of a device object
Write	Allows the ALP service user to modify the value of a device object
Event	Allows an ALP service user to report a device object event
Action	Allows an ALP service user to command a device obj. to execute an action
COS ON	Specialized event services that a reports a change of state to the ON state
COS OFF	Specialized event services that a reports a change of state to the OFF state
Write ON	Specialized write services that a writes an ON state to a device
Write OFF	Specialized write services that a writes an OFF state to a device
Connection	Allows the ALP service user to open/close individual logical addr. connections
Channel	Allows the ALP service user to establish and use Multicast and Peer-to-Peer channels

The SDS service model uses four primitive functions: Request, Response, Indication and Confirm, to provide the Application Layer services. When an initiating device invoke an application layer service (such as the "read" service), the following sequence of events occurs.

- The request primitive is presented to the Application Layer.
- The application layer generates an Application Layer Protocol Data Unit (APDU) to be processed by the Responding Device's application layer.
- The Application Layer issues a send message request to the CAN Data Link Layer using the APDU.
- The Data Link Layer prepares a CAN-formatted Protocol Data Unit (PDU) and presents it a bit at a time to the Physical Layer for sending to the Responding Device.
- The indication primitive represents the requested service as it is received at the Responding Device's application layer.

The Responding Service User creates a response to the read request.

- **The response primitive conveys the information from the Responding Device.**
- **The confirm primitive notifies the Initiating Device that the response has been received.**

The Mupaac implementation of the Smart Distributed Systems Service Model is a reduced implementation of the full SDS protocol, it uses all the four primitive functions: Request, Response, Indication, Confirm. All two service conventions are implemented: Basic and Fragmented. In Mupaac-SDS are implemented only three Application Layer services:

- **READ**
- **WRITE**
- **ACTION**

READ Service

The Read Service is used to read an attribute value of an Embedded object. For example, this service could be used to read the present value of a sensor.

WRITE Service

The Write Service is used to modify an attribute of an Embedded object. For example, this service could be used to set an actuator output to on or off.

ACTION Service

The Action Service is used to execute the actions specified for an Embedded object. For example, this service could be used to move an axis to a target position.

PCI BUS: hardware and software issues

Before to discuss what will be done for the PCI bus, it is better to explain why the PCI is capable of satisfying our requirements in terms of performance and thus why we have chosen to use it.

The main data exchange between SIPC and DSP boards is due to the passing of macropoints to DSP-PCI boards. As previously stated the maximum number of DSP-PCI boards is not fixed, since it depends on the performance required by DSP-PCI boards.

For example, if a system presents 32 axes at least 4 DSP-PCI boards must be used (no more than 8 axes per board), with a refresh time = 500 micro sec. A faster refresh time can be obtained by increasing the number of DSP-PCI boards: 8 DSP-PCI boards with 4 axes and a refresh time of 250 micro sec.

From the point of view of the communication between PC and DSP-PCI boards, if an architecture with 8 DSP-PCI boards with 4 axes each is chosen, then the SIPC has to pessimistically send about 400 bytes to each DSP board and to receive back about 100 bytes (error values, signals of synchronization, etc.). In the 400 bytes the macropoints, the parameters of trajectory, etc. Thus 500 bytes for each board every 250 micro sec leads

to need 2 Mbytes per seconds per DSP board. If 8 DSP boards are present, then 16 Mbytes of throughput are needed.

In the above cases, the PCI bus has no problems, since it can reach without any problems even 33 Mbytes per second in burst mode (by using the right chip set). Moreover, the use of PCI in industrial context is rapidly growing (see Ventura Development review), and it is reasonable that it will become in few years the most commonly used bus. The DSP chip on DSP-PCI board will be interfaced to PCI bus by using a dual memory. Therefore, we have 125 byte/axis to transfer, a minimum refresh time of 125 micro sec and a maximum of 20 Mbytes per second of throughput for the PCI (see next Section).

Please note that if more complex interpolation mechanisms will be used in MUPAAC systems a maximum of 1 Kbytes of data for each board will be required (e.g., cubic splines, nurbs, B-splines), then 4 Mbytes per second will be needed. In this case there are two possibilities:

- the reduction of the number of axes per DSP board, or
- the reduction of the number of DSP boards for SIPC.

Both these solutions are possible since MUPAAC architecture is flexible as it is shown in the next subsection.

High Level PCI Protocol

The protocol used for communication of the SIPC and the DSP boards is simple and efficient. The DSP-PCI interface provides a memory mapped common data region, this region is subdivided in two parts. One is used for communication from SIPC to DSP and the other for communication from DSP to SIPC.

Since the common memory is of 32KB, and 16KB is used for transferring messages in one sense and the other 16KB for the other sense one message may be approximately up to 16KB long. The subdivision of the memory in two equal parts may be changed if during test phases will be seen that different amount of memory are needed.

The communication is handled through interrupts; there are two specific location in the common memory that when they are accessed generate interrupts one to the SIPC and one to the DSP.

The communication protocol for transmission of the message from the SIPC to the DSP is:

1. The SIPC writes the message in the SIPC2DSP memory zone at a specific address (every board has a different address).
2. The SIPC accesses to the location to generate the interrupt to the DSP.
3. The DSP when receives an interrupt reads the message.
4. The DSP produces an ACK message in the DSP2SIPC memory zone at a specific address.
5. The DSP accesses to the location to generate the interrupt to the SIPC.
6. When the SIPC receives the interrupt for an ACK message the communication is ended with success. If the interrupt is not received within a certain time-out the interrupt to the DSP is regenerated and this procedure is repeated for a maximum number of times after which the communication is ended with fault.

The other type of communication is perfectly symmetric.

The communication protocol for trasmission messages between SIPC and DSPs can be synchronous or asynchronous, there are some messages that not require an ACK message. For example, when the DSP has executed all the instruction, the DSP sends an interrupt to SIPC to indicate the end of instruction. The SIPC when receives this type of interrupt decides to send new instruction (if there are other instruction to execute) or if there aren't instruction don't answer.

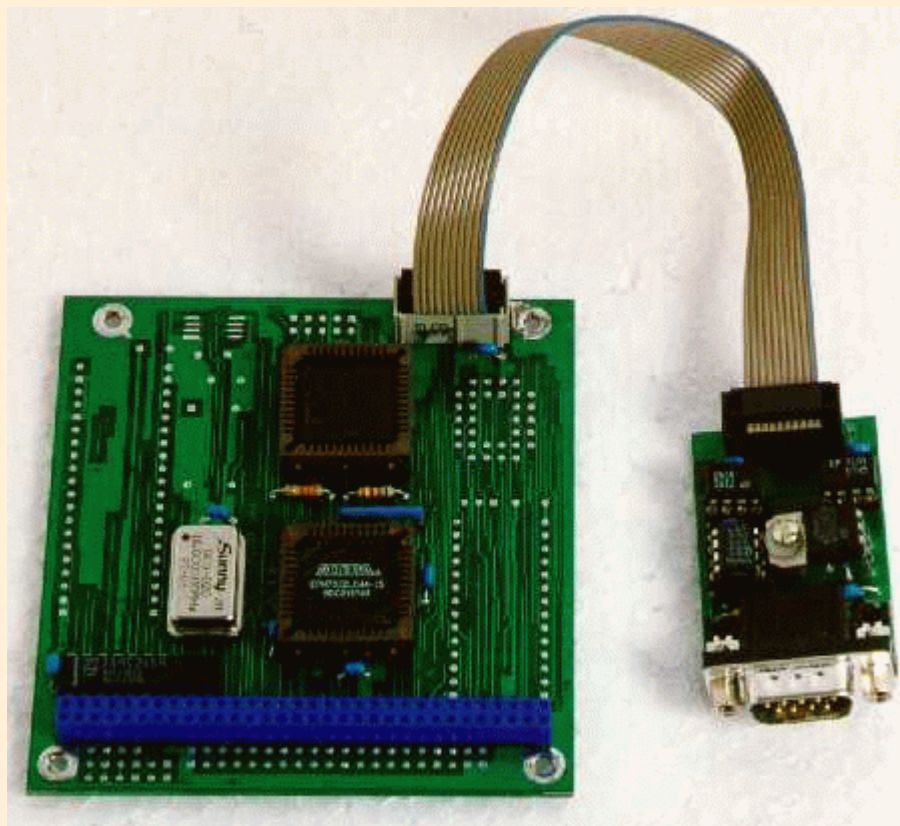
Details about MUPAAC Components

PC-CANBUS board

PC-CANBUS board will be built for EISA bus, PC104. This board will be installed in the PC machine, which is used (i) to enter the ISO program, (ii) supervising the work of the several SIPC boards which can be present on the network, and (iii) connecting the area to other areas by means of an Ethernet network.

The PC is also the main user interface of the system. The PC is connected with at least a SIPC, and sends commands to it, but also receives information and alarms from it. The PC is a commercial industrial personal computer endowed with EISA bus, PC104.

When the architecture requires to communicate to the SIPCs of the architecture more than 500 Kbs this board is substituted with an Ethernet at 10 Mbps or 100 Mbps depending on the requirements.



SIPC board

SIPC board is the most important component of MUPAAC system. In fact, its services are:

Reception and interpretation of ISO instructions sent by the PC. On the basis of the program received, SIPC manages all other devices which compose the CNC: DSP-PCI boards (i.e., axes) and I/O boards (i.e., I/O ports). SIPC also sends information to PC for synchronising other SIPCs and for advertising of the presence of alarms.

- Transmission of elaborated information to each DSP-PCI board:
- macropoints and data useful to calculate micropoints (by means of interpolation),
- control commands, and
- other general parameters.

Moreover, each DSP-PCI board returns reference coordinates to SIPC for synchronization with other axes and alarms.

- Resolving logic equations and:
- producing messages to input boards and ports, and
- acquiring data from output boards and ports.

Therefore, SIPC board could present

- two CANBUS interfaces and one PCI interface, or
- a CANBUS interface and an Ethernet interface and a PCI interface.

The SIPC board presents: a CPU (Intel Pentium, or Pentium pro), main memory (from 8 to 32 Mbytes of RAM), EPROMs for bootstrap and containing the specific software, 1-2 CANBUS interfaces, a PCI interface (called SIPC-PCI interface), a specific local bus for connecting this board to a video adapter, a keyboard, an RS232, a disks, and optionally an Ethernet board, etc., for allowing the full test and debug. The operative system has to be a specific ROMable kernel as in the present INDEX-DSP architecture.

Please note that, differently from INDEX-DSP main board, the SIPC can be connected with more than one DSP-PCI board. The maximum number of DSP-PCI boards for each SIPC depends on the throughput of PCI network and on the request of data of these DSP-PCI boards. For example, a typical SIPC has 4 DSP-PCI boards for managing at most 16 axes simultaneously (4 axes for each DSP-PCI board). The SIPC must manage a greater number of I/O ports than INDEX-DSP (max 8 axis on a single DSP board and max 60 I/O ports for all). It is reasonable that a CNC system needs about 5 bits (I/O ports) per axis, thus MUPAAC will manage about 40 bits (5 times 8) of I/O for each PCI-DSP board installed. If 4 DSP-PCI boards with 8 axes each are installed, thus 160 bits are needed. In certain cases, also other types of I/O ports can be needed, for example bytes, analog data, etc. In general, no more than 256 bits are needed in the above conditions.

Another limitation for the SIPC board is the number of the so-called blocks to be generated on basis of the ISO instruction interpreter and macropoints generator (see Fig.3). For an 80486 DX2 66 the number of blocks processed per second is about 300, these are enough for satisfying the needs of 8 axes at 250 micro sec or 4 axes at 125 micro sec and so on. MUPAAC will provide a stronger microprocessor (e.g., Pentium Pro 200 Mhz) thus SIPC board will be capable of processing at least 1200 blocks per second.

Card SIPC is the controller of system MUPAAC. The aim of this project is to obtain a high performance architecture for control at low costs. For these reasons, it has been decided to use of the microprocessors of the family Intel Pentium. The realization of a mother board, that supports that kind of

microprocessors, is a time consuming project. It is faithful for the capacity of the team of MUPAAC, but obviously out of the scope of this specific Activity which is mainly devoted to exploit HPCN technology. For these reasons, and in order to reach the objectives proposed: for producing a prototype in few months we decided to implement SIPC board to get material from the market. According to the Exploitation Plan, once obtained and tested the MUPAAC prototype a specific SED mother board will be built -- that is, after the completion of project.

In the market there exists several boards that can be profitably used as SIPC -- e.g., MITAC, INSIDE, AMD. More specifically these are simply PC boards for passive bus. They have to be considered a full SIPC only when they present the PC-CANBUS board the related software as discussed above.

In particular, the SIPC board has to provide a PCI interface and a PC104 bus, obviously memory etc. The PC 104 is used for expanding memory, Ethernet card, for the PC-CANBUS board, for the optional graphic user interface, etc.

It has been chosen to use a Ethernet protocol between Pc and the several subsystems, so as to be able to obtain a twofold advantage, a wider bandwidth regarding the plan originally previewed with only a CANBUS. This solution is also much more interesting for the purchasers that have an already installed Ethernet network in the factory. The use of the Ethernet for connecting subsystems will allow to have a lower price for the total system, and therefore a wider spread of the product.

DSP-PCI board

A DSP-PCI board is responsible for the coordination of the motions of at most 4 axes. This maximum number of axes depends on the number of analog input and output ports which are directly managed by the DSP-PCI board for providing the action on motors and the reading of sensors (i.e., position, velocity, etc.). Each DSP-PCI board provides the following services:

- reception of commands from SIPC board by means of the DSP-PCI interface;
- the calculation of micropoints. This is done interpolating macropoints sent by SIPC board; as in INDEX-DSP, three interpolation types (linear, circular and spline) will be available on MUPAAC. The DSP-PCI board uses micropoints to evaluate action values for axes (using specific analog outputs which are placed directly on DSP-PCI board), in order to produce the required trajectory;
- evaluation of the actions for the motors of axes on the basis of the data read by means of specific analog inputs ports. The control is based on PID (Proportional Integrative and Derivative) algorithm plus additional filters for reducing problems due to machine characteristics (these are need to allow the reaching of high velocity and precision).

These elaborations require a high calculation power; as in INDEX-DSP, a DSP will be used (Analog Device AD 2181) (DSP offers high speed at low cost). The other parts of these boards (for example axes control) will be fully derived from those of INDEX-DSP. The PCI interface will substitute a method based on dual memory implemented in INDEX-DSP where only one DSP board for main board is allowed.

DSP-PCI board will be capable of evaluating action values for axes every 250 micro sec (if 4 axes interpolated are used); lower or higher values could be set when performance required are higher or lower, respectively. For example, limit values will be 500 micro sec for 8 axes, 125 micro sec for 2 axes. As conclusion, the limit of this board is = 125 micro sec and the number of axes ≤ 8 axes. Moreover, the ratio between the refresh time and the number of axes (T/NA see Tab.1) must be = 62.5 (micro sec per axis); thus 1000 micro sec for 8 axes is allowed. Other examples of complete configurations will be given later.

This board is the core of the hardware of the project. In fact this board has to control the correct positions of axes of the connected machines. For the choice of the microprocessor to be used in the DSP-board, three DSPs have been evaluated. The choice has been limited to these DSPs since the power required and

the dimension of the memory required do not leave space to add more DSPs:

- Motorola 5630x
- Texas Instruments TI320C3x
- Analog Device AD2106x (SHARC)

The Motorola's chip, is the only one (of the three) with a built-in interface to the PCI bus, but it has been discarded because it does not provide a floating-point unit. The experience made with the INDEX-DSP project suggested that all components without a floating-point unit should be avoided.

The choice between the chips of Texas and of Analog Device, has selected the Analog Device processor although it has a greater price. The main reasons for this choice are as follow:

- A greater power of calculation; The Analog's DSP has a power of 120 Mflops whereas the Texas's DSP has "only" 60 Mflops.
- A more reliable evolution since it has been recently proposed;
- High flexibility in its use. The development toolkit of the Analog Device DSP is simpler to be used with respect to that of Texas.

The selection has been made on the basis of objective experience since DIE has a direct experience on TEXAS DSPs while DSI and SED have a direct experience on Analog Device DSPs.

More discussions, tests and benchmarks have shown that the difference, in terms of performance is greater than that shown by the simple velocity index introduced above. The greater performance of the Analog's chip follow from its capacity to compute the same program with a number of elementary instructions lower than those used by the Texas's chip.

The Texas components family is on the market from many years, in 1997 Texas presented a new component (not yet available) with technical characteristics better than those of the TI320c3x family, but with a price that will be similar. This could lead Texas Instruments to abandon the production of the more obsolete component.

For the MUPAAC project seems that the large serie production could not begin before two years (one year for design and realization, one year for the introduction of the new product in the market). For SED should be a great damage if after to have planned and realized a system based on the TI320c3x, this came removed from the market.

On the contrary the Analog's DSP has been presented recently. Moreover, Analog Device is developing new products on the same line, for this reason seems that we can expect a product stability for more years. Moreover the relative youth of SHARC can lead to suppose, with reasonable security, a decreasing price.

The last reason, but not the least important for the choice of the DSP, has been its scalability. In fact the SHARC family is composed of three chips, all pin-to-pin compatible. For this characteristic a board based on these family can be easily adapted to different needs.

For these reasons has been decided to use for the DSP-PCI board a microprocessor of the AD2106x family, in particular to the current state of the market, the AD21061 seems to be the best choice for our needs.

On the base of the experience made with the INDEX-DSP project, seems that can be sufficient 256 Kbyte of RAM memory, besides those already present on

the AD21061 (128Kbyte).

The interface between the DSP board and the board named SIPC through the PCI bus will be made with a double port memory with 32 bit parallelism and a deep of 2 Kbyte.

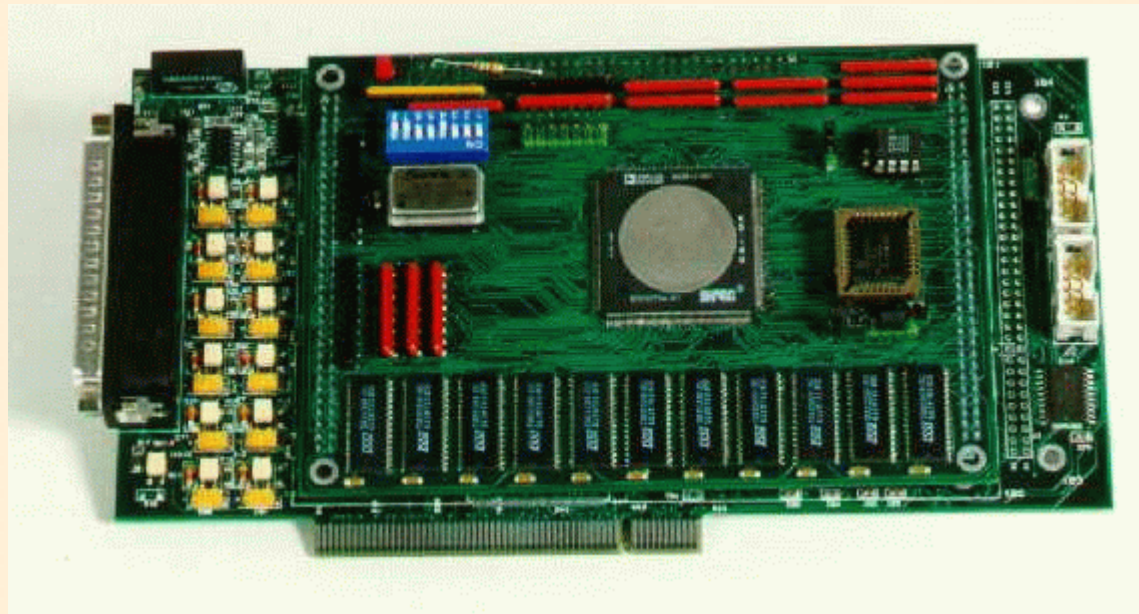
Moreover, an EPROM memory of 512 Kbyte is needed for the code and an EEPROM memory of 32 Kbyte to save some parameters of the axes managed by the board. For the EPROM and EEPROM will be used memories with 8 bit parallelism, since the access to these memories does not influence the overall performance of the machine.

Since the DSP-PCI board has to control four axes, it needs four D/A converters. The DACs selected have 6 bits of resolution, a such high resolution is due to the necessity to obtain a system that uses all the potential calculus capacity that the machine offers.

For the interface with the encoders, the needed logical functions will be made with an EPLD, this is mainly due to economic reasons, with respect to the use of specialized components.

To obtain a great flexibility for the system, on the DSP-PCI board, also four A/D converters with 10 bit resolution, a RS232 serial port, a CANBus communication channel, four digital outputs and eight digital inputs have been included.

The interface between the DSP and the PCI bus will be realized through the implementation of the needed logical functions with an EPLD. This will permit to SED to obtain a deeper knowledge on the PCI bus rather than that obtainable from the use of specific chips. Moreover this will bring to a product adaptable to various needs. Another advantage is to have a product surely stable in time that has not to deal with the high variability of the PCI chip interface market.



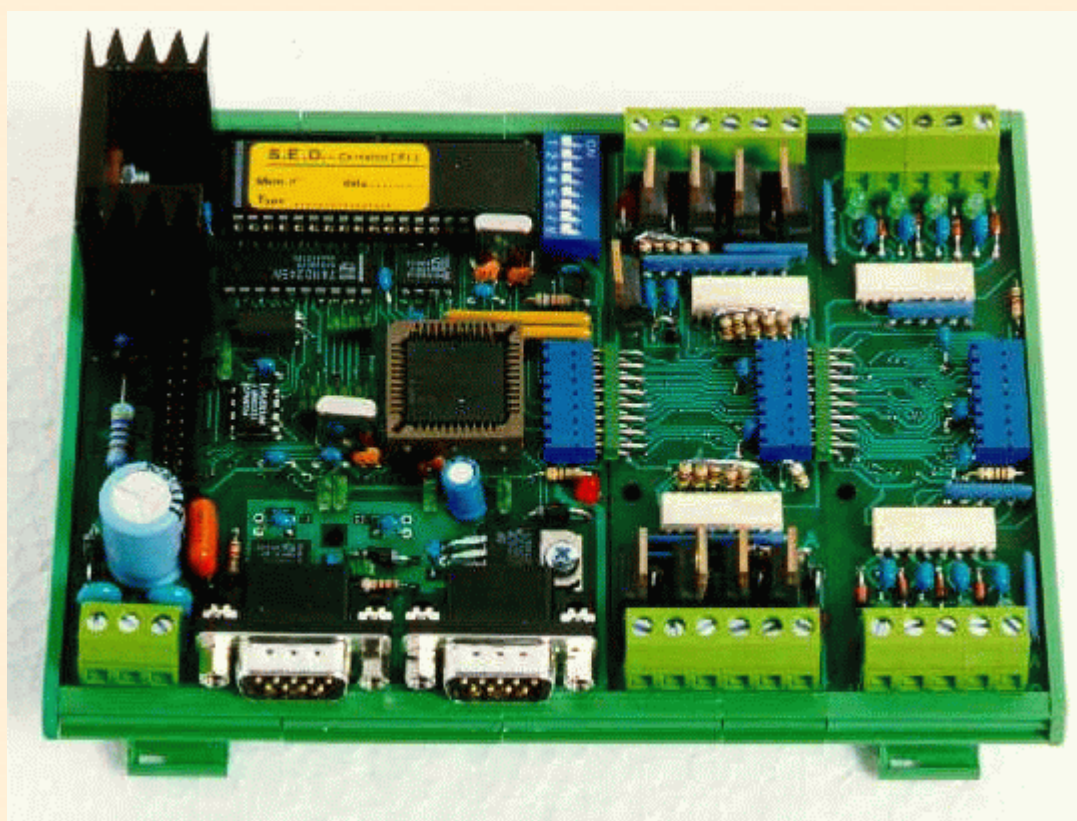
I/O Boards

These I/O boards are quite simple. They will present a very simple microprocessor for embedded system -- i.e., an Intel 8051. Its work consists in:

- receiving commands from a specific CANBUS chip and thus from SIPC via CANBUS;
- interpreting the corresponding commands;
- executing the commands which can be: read/write of the internal status, read of an input port, write of an output port.

Presently, SED produces several types of I/O boards. Examples are boards for providing: 16 digital inputs and 16 digital outputs, 8 digital inputs and 8 digital outputs, 32 digital inputs, 32 digital outputs, 16 analog inputs (12 bits), 32 analog inputs (8 bits), 4 analog inputs (16 bits), 16 analog output (12 bits), etc. Digital and analog ports are available with different voltages, with and without isolation, etc.

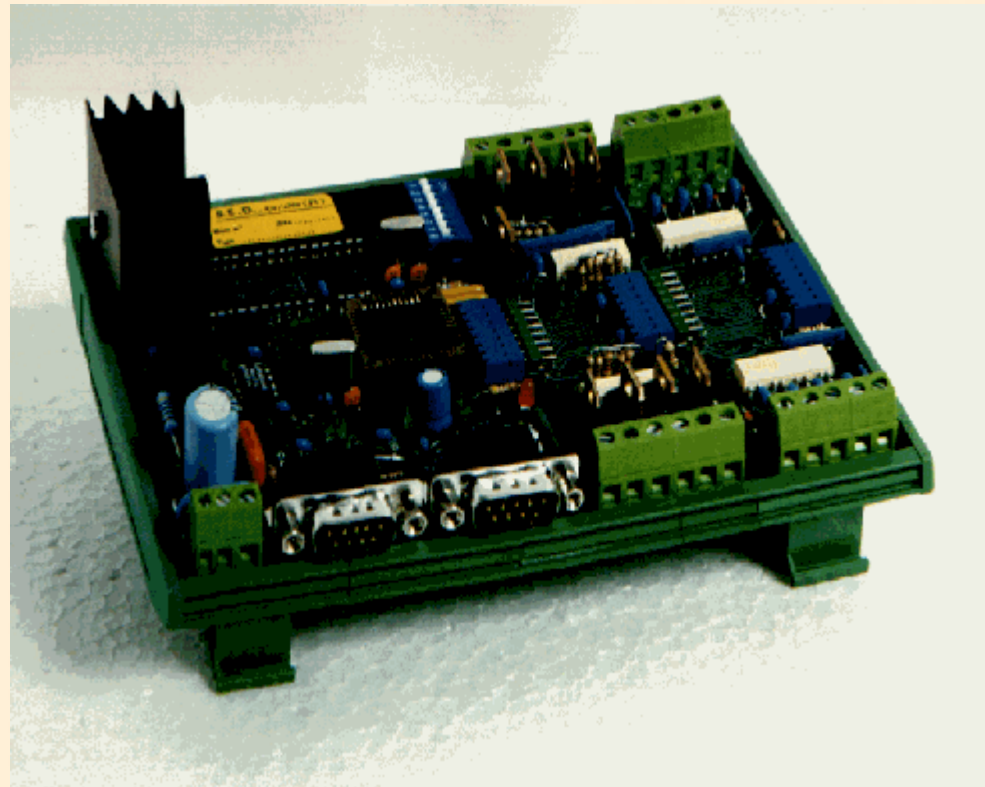
Two kinds of CANBUS modules will be produced: one provided of a CPU while the second will be completely passive.



I/O CANBUS module with CPU

This module could be realized with a cpu of low price (Intel 8051) for the realization of modules with a limited needs of calculation power, or with a more powerful microprocessor (Hitachi SH7000), in the case the customer needs to manage many modules in complex configurations.

An example of an I/O canbus module is shown in the picture below.



It is composed of:

- A CPU Intel C51 (a very low cost CPU);
- A SPI-module with 8 digital OUTPUT;
- An SPI-module with 8 digital INPUT TTL.

We can add many other modules like analogic input, output with relais, counter or monoaxes controller.

I/O CANBUS modules

Inputs/Outputs

8 digital inputs 24 V a.c.

8 digital outputs with relays

8 digital inputs 24 V c.c.

8 digital outputs with transistor

Converters

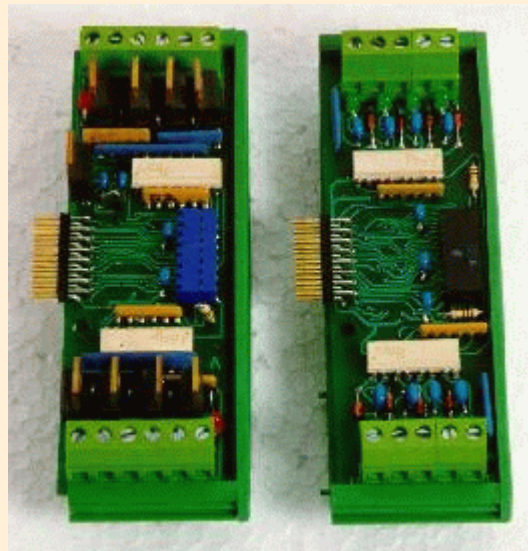
1 A/D converter 12 bit multichannel

1 A/D converter 12 bit monochannel conditioned

Various

1 counter with 2/4 channels 32 bit

1 module for the management of single axis



Flexibility of MUPAAC

As a conclusion the main differences between INDEX-DSP and MUPAAC architecture are summarized in Tab.1.

Features	INDEX-DSP	MUPAAC
SIPC-DSP communication	shared memory	PCI
PS-SIPC communication	RS 232	CANBUS
SIPC-I/O communication	Logipack, RS485	CANBUS
maximum number of main boards	1	10 SIPC boards
maximum number of DSP boards	1	depending on performance
maximum number of axes per DSP board	8	8
minimun refresh time for 2 axes	125 microsec	125 micros
minimun refresh time for I/O	15 millisec	10 millisec
control algorithm	PID	PID

Tab. 1: INDEX-DSP vs MUPAAC, limits and features

In Tab.2 a set of possible configurations of MUPAAC architecture are presented. The configurations present from 4 to 128 axes and performance from 125 to 1000 microsec as period for updating actions of control on axes. Lower performance are also possible but they are out of the goal of MUPAAC architecture as previously stated.

Case	# Ax	Ref. Ax.	T/NA	# DSP	# Ax/DSP	PCI B	Block/s	#SIPC	#DSP/SIPC	C
1	4	125	31.25	2	2	4	600	1	2	4 (2+2)
2	4	250	62.5	1	4	2	300	1	1	2 (2+1)
3	4	500	125	1	4	1	150	1	1	2 (2+1)
4	4	1000	250	1	4	0.5	75	1	1	2 (2+1)
5	4	2000	500	1	4	0.25	37.5	1	1	2 (2+1)
6	8	125	15.62	4	2	8	1200	1	4	6 (2+4)
7	8	250	31.25	2	4	4	600	1	2	4 (2+2)
8	8	500	62.5	1	8	2	300	1	1	2 (2+1)
9	8	1000	125	1	8	1	150	1	1	2 (2+1)
10	8	2000	250	1	8	0.5	75	1	1	2 (2+1)

11	16	125	7.81	8	2	16	2400	2	4	12 (8+4)
12	16	250	15.62	4	4	8	1200	1	4	6 (4+2)
13	16	500	31.25	2	8	4	600	1	2	4 (2+2)
14	16	1000	62.5	2	8	2	300	1	2	4 (2+2)
15	16	2000	125	2	8	1	150	1	2	4 (2+2)
16	32	125	3.9	16	2	32	4800	4	4	24 (8+16)
17	32	250	7.81	8	4	16	2400	2	4	12 (4+8)
18	32	500	15.62	4	8	8	1200	1	4	6 (2+4)
19	32	1000	31.25	4	8	4	600	1	4	6 (2+4)
20	32	2000	62.5	4	8	2	300	1	4	6 (2+4)
21	64	125	1.95	32	2	64	9600	8	4	48 (16+32)
22	64	250	3.9	16	4	32	4800	4	4	24 (8+16)
23	64	500	7.81	8	8	16	2400	2	4	12 (4+8)
24	64	1000	15.62	8	8	8	1200	1	8 NP	10 (2+8)
25	64	2000	31.25	8	8	4	600	1	8 NP	10 (2+8)
26	128	125	0.97	64	2	128	19200	16	4	96 (32+64)
27	128	250	1.95	32	4	64	9600	8	4	48 (16+32)
28	128	500	3.9	16	8	32	4800	4	4	24 (8+16)
29	128	1000	7.81	16	8	16	2400	2	8 NP	20 (4+16)
30	128	2000	15.62	16	8	8	1200	1	16 NP	18 (2+16)

Tab.2: #Ax. is the number of axes of the system; Ref.Ax. is the refresh time in microsec for evaluating the action on axes; T/NA is the ratio Ref.Ax/#Ax; #Ax/DSP is the number of axes per DSP-PCI board; #DSP is the number of DSP-PCI boards in the whole system; PCI B is the general throughput on PCI in Mbytes per second which is evaluated considering 125 bytes/axes multiplied by #Ax. and divided by Ref.Ax. in microsec; Blocks/s is the number of blocks which have to be processed per second; #SIPC is the number of SIPC boards with #DSP/SIPC DSP-PCI boards each; #DSP/SIPC is the number of DSP-PCI boards for each SIPC board (#DSP/#SIPC); and C is a cost factor evaluated considering the cost of SIPC double with respect to that of DSP-PCI board.

Please note that in Tab.2: #DSP is evaluated considering also that each DSP-PCI board can support at most 8 axes, #SIPC is evaluated considering that PCI bus can support at most 16 Mbytes per second and each SIPC can produce at most 1200 blocks per second.

As it has been shown the MUPAAC architecture is flexible since can be fully reconfigured for satisfying the requirements of the pipeline of production. It can be suitable for covering both low level architectures (at low cost) and high performance control networks. Moreover, additional axes, DSP-PCI boards, SIPC boards can be added/removed when needed/unuseful. Obviously, all inter-medium configurations in which different DSP-PCI boards work by using different values of Ref.Ax. are possible according to the machine under control.

As it can be observed by column C of cost index (which can be obviously considered also a price index) the cost is directly proportional to $(T/NA)^{-1}$ factor. This can be also considered a measure of the performance required by the automatic control, lower values are related with higher performance which is linear with the number of axes. The above presented progression for the cost/price is linear with the performance while the

others control builders present a geometric progression of price with the increment of performance. Moreover, C presents also a linear behavior with the number of axes for high performance configurations while for low performance configurations (2000 Ref.Ax.) the cost per axis decreases with the number of the axes. For these reasons, the final price for medium and high performance MUPAAC configurations will be lower than those which have been reported for the other similar solutions.

Also INDEX-DSP presents a geometric progression of cost/price with the increment of this $(T/NA)^{-1}$ factor. This is mainly due to the need of a main board every 2/4/8 axes, thus 64 axes mean at least 8 main boards. Therefore, for INDEX-DSP the cost index is obtained by using $C = 3 N.Ax./2$ (if Ref.Ax. is 125 microsec m only two axes can be controlled per DSP board); thus for 64 axes $C=96$ instead of 48 for MUPAAC. Another example: if Ref.Ax. = 1000 microsec , then $C = 3 N.Ax./8 = 48$, with 8 axes for each INDEX-DSP. In these evaluations, a scale factor of 3 has been used since each INDEX-DSP control presents one main board and one DSP board. This demonstrates the strong reduction of cost/price that the HPCN technology will produce on SED products. Especially for configurations and products presenting high performance and technology. The reduction of cost/price and the flexibility will be capable of increasing of 30 % of the number of automatic controllers sold by SED. Moreover, it is been also estimated to have an increment of 10 % for the acquiring of a new piece of market of the high-performance controller for the proposition of cheaper controllers (at the same performance) with respect to those which are available on the market.

Planned Results

The major objective of MUPAAC activity is to insert HPCN technology in SED and within the builders of several automatic machines for cutting, soldering, etc., matter in FMM and FMC working areas. These end-users are mainly SMEs in which no distributed/parallel systems for controlling their equipments are present. The adoption of HPCN technology will allow the providing of new functionalities and business benefits for both end-users (machine builders, i.e., VALIANI) and technology transfer receivers (i.e., SED). The activity has the following specific objectives:

- **introducing HPCN technology for building, on the basis of already available computerized control of SED a flexible and reconfigurable parallel/distributed system for control in order to reduce the costs/prices for the machine builders of about 20 %. The system has been considered strongly needed for (i) integrating automatic machines into pipeline of production; (ii) allowing the implementation of FMCs at low cost. The solution proposed present several technical and business benefits. The goals are obtained by**
 - **reducing the cost/price of automatic controllers from 20 to 50 % depending on the performance required (compared with the currently produced controllers of SED and with those which are present on the market).**
 - **reducing the costs of maintenance and running: (i) reducing the cost for reconfiguring the pipeline of production, (ii) simplifying the synchronization of machines centralizing the supervising of control.**
-

Dissemination and Demonstration

Disseminating the results obtained at two levels:

National

The partners will presents of their results and experiences in a public demonstration at BIAS in Milan (October 1998) for machine builders with an exhibition stand.

The partners also plan to present their work a national Fair for machine builders.

They also plan to attend some of the next events -- e.g., INTERBIMAL in Milan, IPACK-IMA, SMAU, BIMU and EMO in Milan.

European

The partners intend to demonstrate their results and experiences in 2 public presentations at SED and VALIANI in Certaldo Florence.



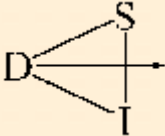



The partners also plan to present their results at the European Fair SACA, and attend/present results to International Fair Elektronica of Monaco, Hannover Messe, Manufacturing Week UK, etc.

Up to July 1998, MUPAAC consortium is ready to give you any kind of technical demonstration in Florence, please contact [Project Coordinator](#).

MUPAAC's Consortium

The consortium includes 5 Partners:

- [SED, SED of Certaldo](#), Prime Contractor and receiver of HPCN technology transfer (Carlo Bruni, Project Coordinator);
- [DSI, Dipartimento di Sistemi e Informatica](#), Università di Firenze, [HPCN technology provider \(Paolo Nesi\)](#);
- [VALIANI](#), industrial firm, one of the most important builders of automatic machines for producing passpartout as end-user (Dr. Valiani);
- [CESVIT](#), partner of TETRApc TTN, disseminator and project controller (Maurizio Campanai);
- [DIE, Dipartimento di Ingegneria Elettronica](#), University of Florence, technology provider (Piero Tortoli).

	SED s.r.l., Certaldo, Firenze
	 Dipartimento di Sistemi e Informatica (DSI)
	Dipartimento di Ingegneria Elettronica
	Valiani S.r.l.
	CESVIT

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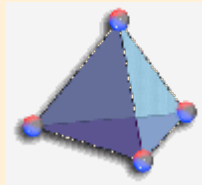
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The Reference TTN

For the ICCOC activity, the partners have chosen to select TTN-TETRApc as their ``reference TTN'' that proposed by CPR (Consortium Pisa Ricerche, Pisa, Italy), CESVIT and CSM. In particular, CESVIT High-Tech Agency (a no-profit agency) has been selected by ICCOC partners as the reference TTN-TETRApc site.

It should be noted that CESVIT for TTN-TETRApc activity collaborates with the Department of Systems and Informatics (DSI partner) which provides support about the technological and scientific aspects of TTN HPCN. This collaboration is very suitable since the complementary roles of CESVIT and DSI within TTN HPCN have been well-identified. CESVIT has a very high visibility and sensitiveness with respect to the market, for distribution, advertising, evaluation, etc. activities (very useful for the management of the TTN-TETRApc), while DSI provides know-how in HPCN technologies (see the enclosed bibliography and biographies, Annex 4). According to the cooperation agreement between CESVIT and DSI for the TTN-TETRApc, the scientific responsible of the CESVIT part of TTN-TETRApc is Dr. Ing. P. Nesi of DSI. Please note that he is also the coordinator of the present activity.



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