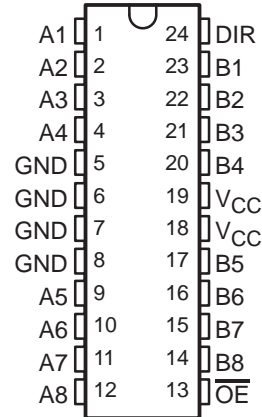


- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic 300-mil DIPs (NT)**

DB, DW, NT, OR PW PACKAGE  
(TOP VIEW)



**description**

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The device allows noninverted data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The 74AC11245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

OUTPUT ENABLE $\overline{OE}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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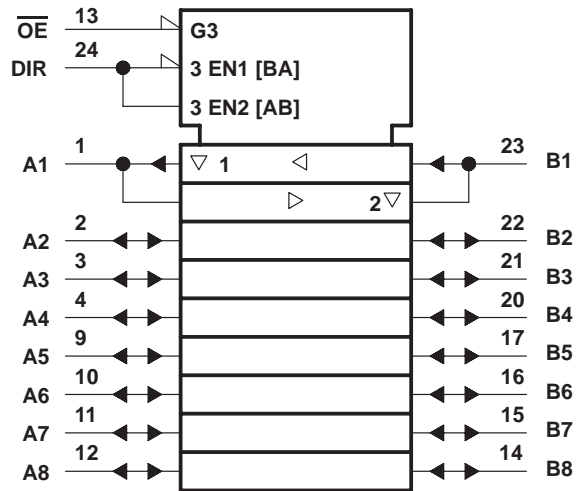
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**74AC11245**  
**OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

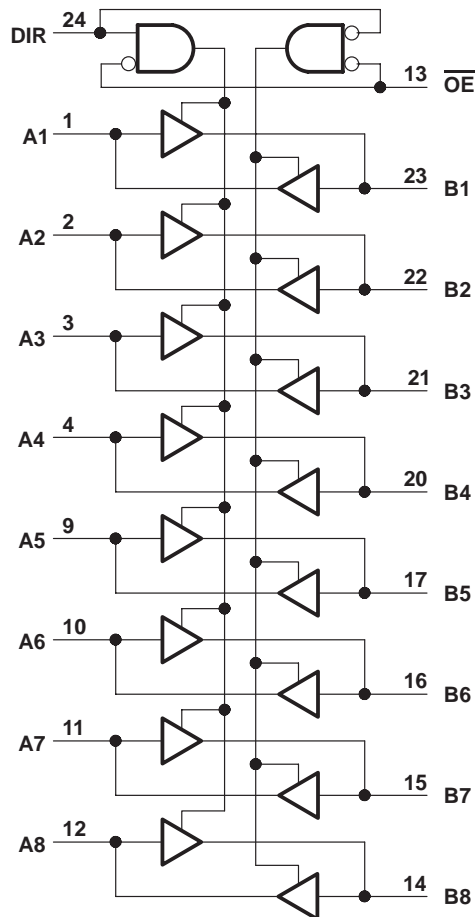
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**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package .....	0.65 W
DW package .....	1.7 W
NT package .....	1.3 W
PW package .....	0.7 W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3$ V	2.1		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 5.5$ V	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3$ V		–4	mA
		$V_{CC} = 4.5$ V		–24	
		$V_{CC} = 5.5$ V		–24	
$I_{OL}$	Low-level output current	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
$T_A$	Operating free-air temperature	–40		85	°C

**74AC11245**  
**OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**  
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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
			MIN	TYP	MAX				
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		V	
		4.5 V	4.4			4.4			
		5.5 V	5.4			5.4			
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48			
		4.5 V	3.94			3.8			
		5.5 V	4.94			4.8			
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V				3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V				0.1		V	
		4.5 V				0.1			
		5.5 V				0.1			
	I <sub>OL</sub> = 12 mA	3 V				0.36			
		4.5 V				0.36			
		5.5 V				0.36			
I <sub>OL</sub> = 24 mA	5.5 V				1.65				
I <sub>I</sub>	A or B ports <sup>‡</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V				±0.5	±5	μA
	$\overline{\text{OE}}$ or DIR						±0.1	±1	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V				8	80	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V				4		pF	
C <sub>io</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V				12		pF	

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	B or A	1.5	6.5	11.2	1.5	12.5	ns
t <sub>PHL</sub>			1.5	5.7	8.5	1.5	9.7	
t <sub>PZH</sub>	$\overline{\text{OE}}$	B or A	1.5	8.6	14.2	1.5	15.9	ns
t <sub>PZL</sub>			1.5	8.2	11.5	1.5	12.7	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	B or A	1.5	7.7	10.5	1.5	11.3	ns
t <sub>PLZ</sub>			1.5	8.5	12	1.5	13	

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

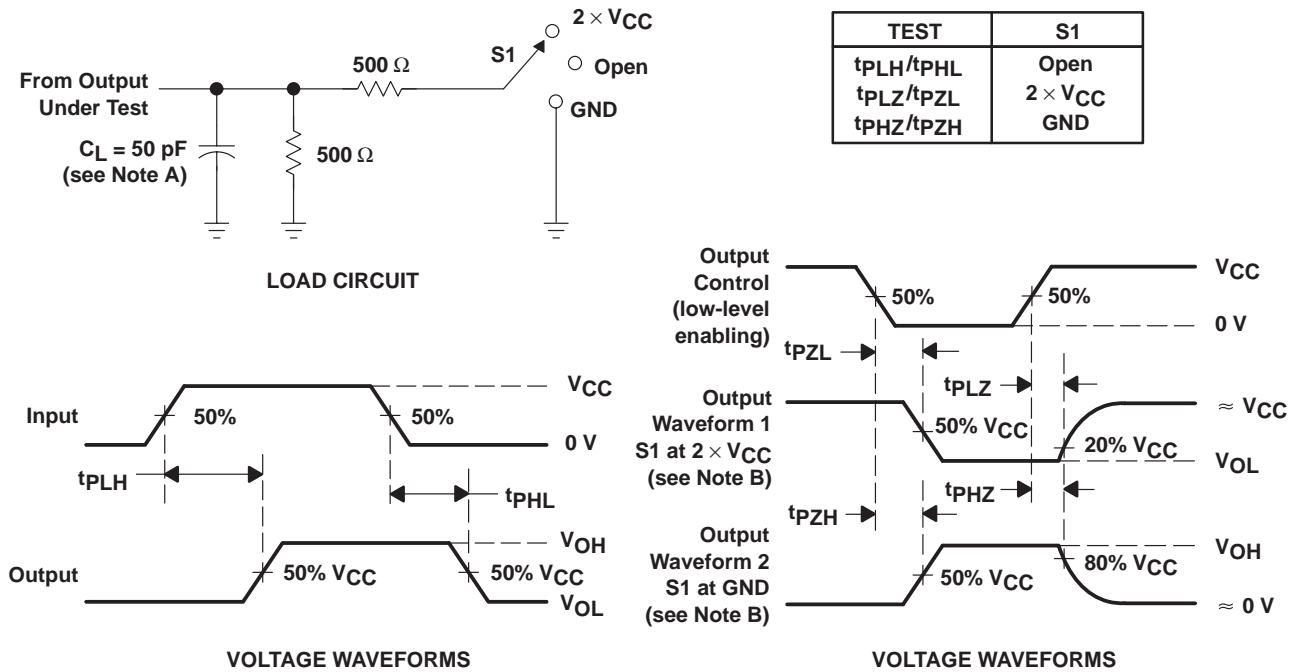
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	B or A	1.5	4.8	8.5	1.5	9.5	ns
t <sub>PHL</sub>			1.5	4.1	6.3	1.5	6.9	
t <sub>PZH</sub>	$\overline{\text{OE}}$	B or A	1.5	6.2	10.2	1.5	11.4	ns
t <sub>PZL</sub>			1.5	5.9	8.6	1.5	9.5	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	B or A	1.5	6.4	8.8	1.5	9.5	ns
t <sub>PLZ</sub>			1.5	7	9.6	1.5	10.4	



operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	64	pF
		Outputs disabled		

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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